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ANALYSIS OF AC TELEMETRY PHASE LOCK CONTROL BOARD

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Table of Contents

SUMMARY v

CONCLUSIONS vi

RECOMMENDATIONS vii

1 INTRODUCTION 1

2 THE PHASE LOCKED LOOP 2
2.1 Phase Detector Block 4
2.1.1 Phase Detectors 4
Diode Ring 4
Exclusive ORs 5
2.1.2 Phase/Frequency Detectors 5
Sample/Hold Detectors 7
Digital Tri-State Comparators 7
2.2 Low Pass Filter 8
2.2.1 Passive Filter 8
2.2.2 Active Filter 10
2.3 Voltage Controlled Oscillator (VCO) 10

3 AC TELEMETRY PHASE LOCK CONTROL BOARD 14
3.1 Voltage Source 14
3.2 Frequency Synthesis 16
3.2.1 Crystal Oscillator 18
3.2.2 Divider Networks 19
3.2.3 Phase Lock IC (MC145152) 21
3.2.4 Integrator 23
3.3 Telemetry Modulation 23

REFERENCES 25

GLOSSARY 26

APPENDIX A - Mathematical Derivations 27

Table of Figures

Figure 1 - Block Diagram - Generic PLL 3
Figure 2 - Operating ranges of a PLL 3
Figure 3 - Schematic Diagram - Diode Ring Detector 6
Figure 4 - Schematic Diagram - Digital Tri-State Comparator 6
Figure 5 - Schematic Diagram - Passive RC Filter ... 9
Figure 6 - Schematic Diagram - Passive LC Filter ... 9
Figure 7 - Schematic Diagram - Second-order Active RC Filter 11
Figure 8 - Schematic Diagram - Third-order Active RC Filter 11
Figure 9 - Schematic Diagram - Modified Pierce Oscillator VCXO 13
Figure 10 - Schematic Diagram - ERL 310414F1 15
Figure 11 - Block Diagram - PLL in ERL 310410F 17

SUMMARY

CONCLUSIONS

RECOMMENDATIONS

1 INTRODUCTION

As the radio spectrum gets more congested and the demand for more accurate frequency selection increases, the phase-locked loop becomes more and more important.
The phase-locked loop (or PLL) provides an easy and accurate method of ensuring that a transmitter or receiver are tuned exactly to the required frequency and remains tuned correctly. This is most necessary when the frequency to be transmitted is in a radio frequency band (RF band) assigned to military forces. If the frequency is even slightly off, unpredictable and potentially dangerous results can be expected.

The PLL was first described in 1932%wy H. de Bellescize [1] but the technology was first used extensively by the American aerospace industry. Now the majority of home, auto and portable stereo systems use PLL technology to provide accurate tuning. What was once an expensive technology is now commonplace.

This report is primarily concerned with the PLL as it is implemented in the AC Telemetry Transmitter (model ETT-) as designed by Emhiser Research Limited (ERL) and manufactured by Emhiser Manufacturing Limited (EML) and Emhiser Manufacturing Inc., Nevada (ERIN). Thus it will not show the uses of the PLL in demodulation of FM and AM signals or in motor control, but rather in the interests of frequency synthesis.

3 THE PHASE LOCKED LOOP

Every PLL circuit has at least two parts: a phase detector (PD) and a voltage controlled oscillator (VCO). In addition to this all but a very few also contain a low-pass filter. The connections between these segments are shown in the block diagram in Figure 1. The basic operation of the PLL is as follows (a more detailed analysis is included later): A reference frequency is inputted into the phase detector which is equal to the desired frequency. The PD compares the phase with the frequency output of the VCO. The output of the PD is an error voltage which is proportional to the difference in phase of the two inputs. This error voltage is filtered so large changes are ignored (as large changes are very difficult to track). The filtered error voltage is the input of the VCO which outputs a frequency which is proportional (ideally) to the voltage inputted. This output is fed back to the PD.

The total effect is that a properly designed PLL will track a signal within a wide range, capture the signal within a narrower bandwidth, and lock the signal within a yet narrower range (See Figure 2). Once the signal has been captured, the PLL will rapidly pull it into the lock range. There is also the necessity to have the signal drawn first into the track zone and from there into the capture zone.

Figure 1 - Block Diagram - Generic PLL

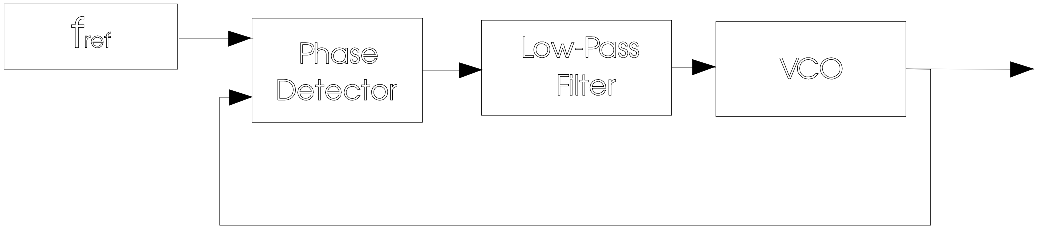
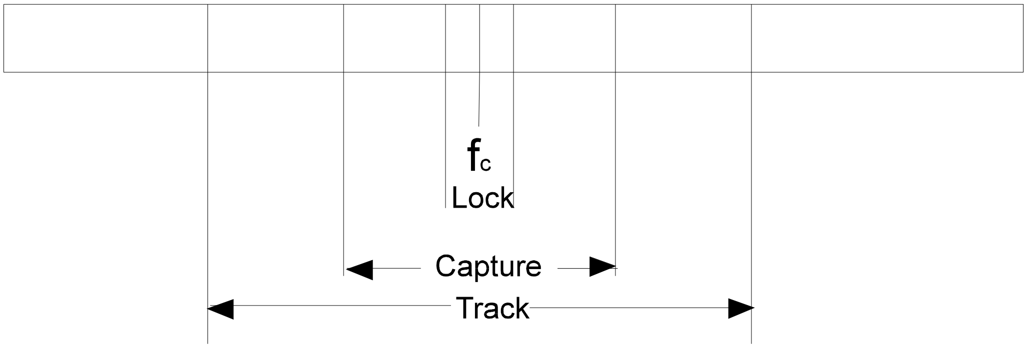


Figure 2 - Operating ranges of a PLL



4.1 Phase Detector Block

There are two types of PDs that are used in PLL circuits. They are the Phase Detector and the Phase/Frequency Detector. When using the Phase detector, there is a necessity to ensure that the VCO is driven to the locking range on power up as the PD will not directly facilitate this. The Phase/Frequency Detector (PFD) is more versatile. If the frequency of the VCO output is lower than the reference, the PFD will apply a higher voltage to the VCO to drive the frequency up, and likewise will drive the VCO down if the output frequency is too high. Once the frequency is correct (or near to it) the PFD acts as a PD.

With either type of detector, the region of operation that is usable in a PLL is where the output is linearly proportional to differences in phase (or at least piece-wise linear).

4.2.1 Phase Detectors

As the use of a plain PD causes the need for a mechanism to drive the VCO into the lock region on power-up, it is more convenient not to use them. Nevertheless, it is worth mentioning the types of plain PDs and their basic characteristics.

Diode Ring

The diode ring (see figure 3) is usually driven with sinusoidal waveforms and also functions as a mixer (when the filter is eliminated). The error voltage is proportional to the phase differences from 90°. The diode ring can only be considered linear when the input signals have constant amplitude and when there are only small deviations in phase. (see Appendix A for mathematical derivation) The main problem with the diode ring is that the output is at most a few hundred millivolts, so it must be amplified causing excessive noise to be added.

Exclusive ORs

The exclusive OR PD uses a single XOR gate to act as a PD for use with digital signals (square waves). This is sufficient as long as the two waveforms have the same duty cycle. If the duty cycles are vastly different, the same output can occur with different phase differences. To avoid this, a pulse stretcher is necessary to make the inputs have equal duty cycles.

Exclusive-OR detectors are usually solely used when the frequencies are high (≥ 1 MHz typically) and close together.

4.2.3 Phase/Frequency Detectors

Phase/Frequency Detectors are usually digital devices (with the exception of the Sample/Hold Detector). These are the devices that are in most common use, partly because of the ease of implementation, and partly because this is the type of detectors that are generally used in the PLL IC's which are very commonly used now.

Figure 3 - Schematic Diagram - Diode Ring Detector

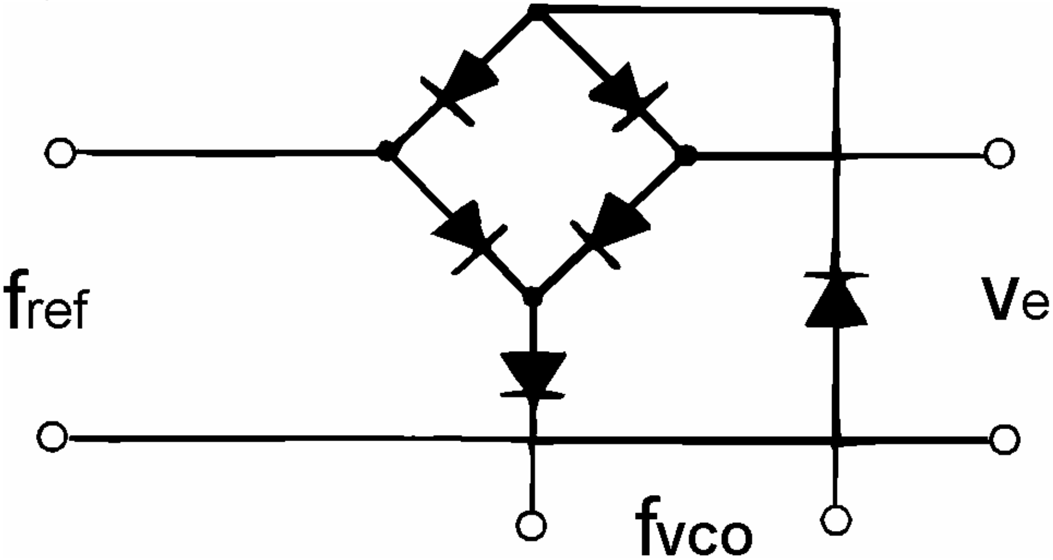
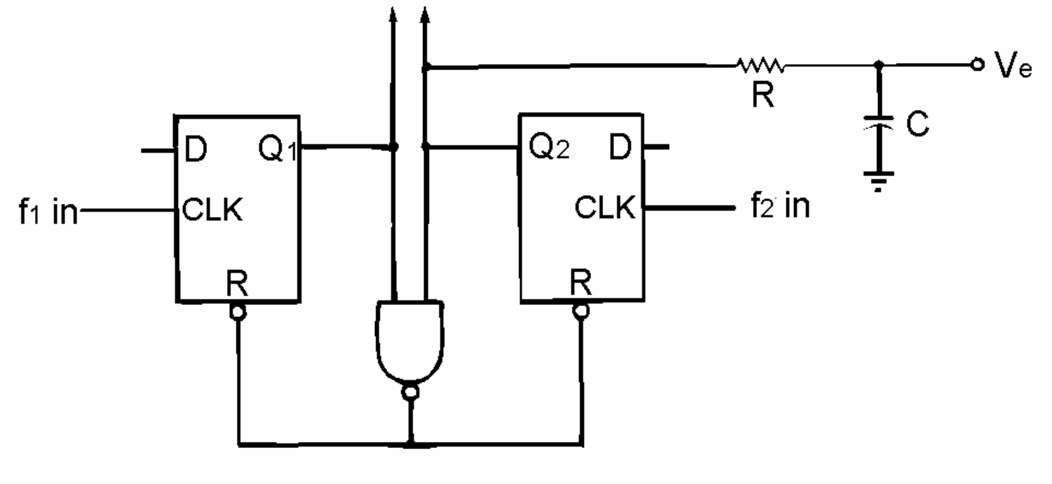


Figure 4 - Schematic Diagram - Digital Tri-State Comparator



Sample/Hold Detectors

Sample/Hold detectors are accomplished with the use of pulse modulation. The analysis of this type of PFD is long and complicated and beyond the scope of this report. The Sample/Hold detectors require filters known as zero-order data hold (ZODH) or boxcar generators. These convert pulse modulated output into a train of pulses with varying width which can be used by the VCO.

Digital Tri-State Comparators

The digital tri-state comparator is the detector that is used in most PLL circuits. The basic tri-state comparator is shown in figure 4. The operation of this detector is as follows: the output of the two D-type flip-flops go high on the leading edges of their respective clock inputs and remain high until both inputs are high when the flip-flops are both reset. If both inputs are of the same phase and frequency, the NAND gate will ensure that the outputs remain low. The two outputs are then connected to an op-amp configured as an integrator (acting as a low-pass filter).

This type of detector is the one that is most commonly found incorporated into PLL IC packages.

4.3 Low Pass Filter

The low pass filter is added to eliminate unwanted harmonics caused by mixing in some detectors. When used with the digital tri-state camparator, its purpose is to convert the current pulses into a ramp waveform that is usable for the VCO. In either case, the filter should be as ideal of an integrator as possible.

There are two basic types of low pass filters: passive and active. The passive filter only includes passive elements (resistors, capacitors and rarely inductors). The active filter adds an op-amp (or rarely transistors) and provides a far superior integrator, thus makes a better filter.

4.4.1 Passive Filter

The passive low-pass filter was the choice of the past as DC amplifiers (i.e. present-day op-amps) were not of very good quality. Now that op-amps present extremely good drift and offset characteristics, this is no longer the case. However, the passive filters do not add noise to the system as all components are passive.

Passive filters do not provide a very good integrator, but nonetheless a passive RC filter (figure 5) is cheap and very easy to make, and thus are still in use. A passive LC filter (figure 6) is either pricey (inductors can cost five to twenty dollars apiece) or difficult to build (if the coils

Figure 5 - Schematic Diagram - Passive RC Filter

Figure 6 - Schematic Diagram - Passive LC Filter

are handmade), but generally create a better integrator than an RC filter.

4.4.3 Active Filter

Active filters have the advantage of being nearly ideal integrators. This means that they perform much better than passive filters in almost all respects. Active filters based on op-amps are simple to make, although optimization often must be done by trial and error.

Typical second- and third-order active filters are shown in figures 7 and 8 respectively. The higher the order of the filter, the more ideal the integrator.

4.5 Voltage Controlled Oscillator (VCO)

The most stable form of VCO in current use (and the only one covered by this report) is the Voltage Controlled Crystal Oscillator (VCXO). A common configuration, a modification of the Pierce crystal oscillator, is shown in figure 9. For highest stability, the crystal XTAL1 in the circuit should be a high-Q ($\approx 2 \times 10^6$), vacuum-mounted, 2.5 or 5.0 MHz, fifth-overtone, AT-cut crystal [5].

This crystal oscillator depends on the crystal functioning as an inductance. This creates a type of LC oscillator in which the variance in frequency is caused by the varactor (or variable capacitance diode) changing the effective

Figure 7 - Schematic Diagram - Second-order Active RC Filter

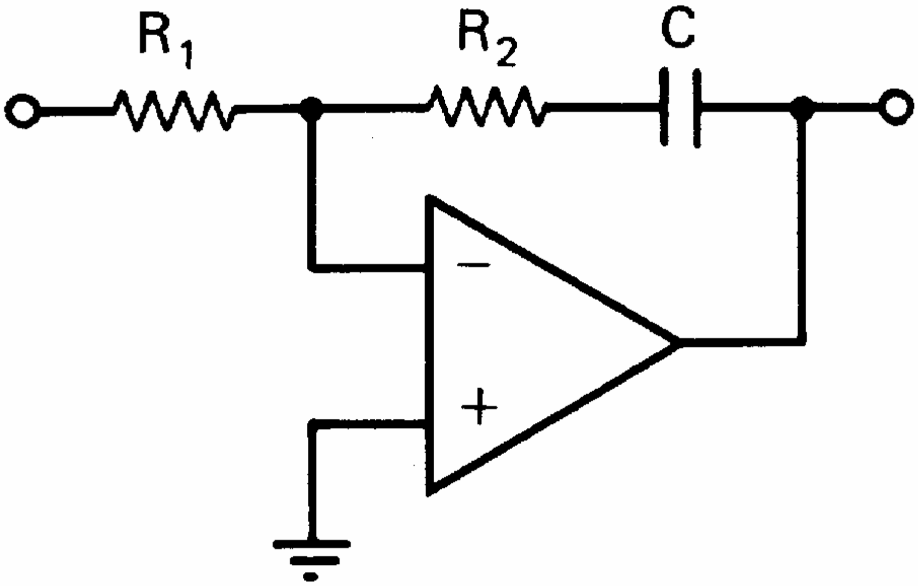
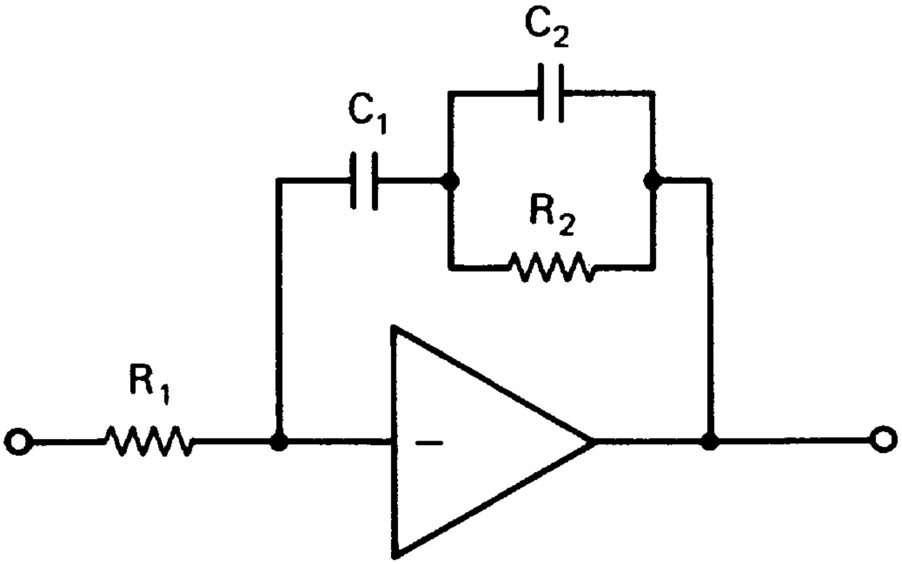


Figure 8 - Schematic Diagram - Third-order Active RC Filter

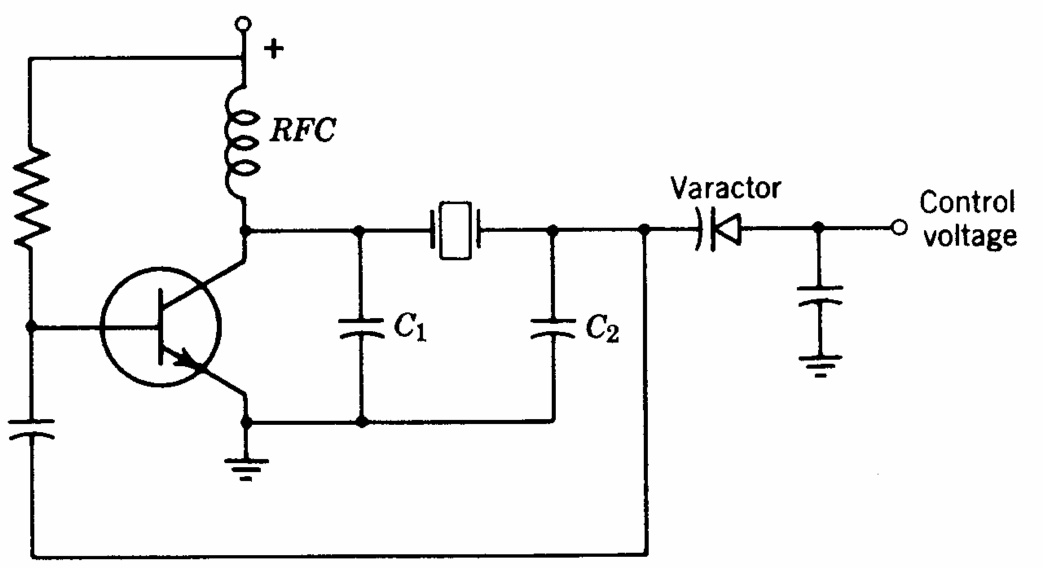


capacitance of C2 as differing voltages are applied to it. As varactors do not vary capacitance over a very large range, the higher the Q (Quality Factor) the crystal posesses, the smaller the tuning range of the VCXO will be. The VCXO shown can only achieve frequencies at or above the fundamental frequency of the crystal.

The RF Choke (RFC) is used to isolate the radio frequency (RF) output from the control voltage input (from the Low-Pass Filter). If this is not done, the high reactances of the crystal and capacitors can cause underirable RF feedback to dissipate into earlier stages of the VCO. This is especially crucial if the output frequency of the VCXO is very high (≥ 100 MHz or so).

The transistor utilized in the VCXO should be as low-noise as possible to minimize the noise on the RF output. To obtain the best signal-to-noise ratio (SNR), it is imperative to operate the circuit at the highest RF level that will not drive the crystal into its non-linear region. Typically, VCXOs are made to output between 10 and 500 μW (much lower than the rated maximum power for the crystals) as these power levels are often found to be optimum [5].

Figure 9 - Schematic Diagram - Modified Pierce Oscillator VCXO



5 AC TELEMETRY PHASE LOCK CONTROL BOARD

The analysis of the AC Telemetry Phase Lock Control Board was to be the main focus of this report, but to accomplish this a description and brief analysis of the PLL was necessary.

The AC Telemetry Phase Lock Board (herein referred to by its part number - 310410F) is one of the simplest PLL control boards designed by Emhiser Research Limited. The number of parts in the circuit is approximately 150 (as compared to about 400 for some of the more complex PLL control boards). The board itself is about 2" x 3" (about 50 mm x 75 mm), a small size that is a dictated by the size requirements of the transmitter it is part of and also by the extremely high frequency of operation (between 2200 MHz and 2300 MHz).

The main sections of the board are: the voltage source for the rest of the transmitter, the majority of the PLL circuit (including the local crystal oscillator, the multimodulus divider, phase lock IC and integrator) and the circuitry providing the telemetry modulation (Frequency modulation) to the loop. These can all be seen on the schematic diagram (Figure 10).

6.1 Voltage Source

The voltage source for the rest of the transmitter is supplied by the 310410F as it is the largest board in the transmitter and because it was put right next to the power connector. Most of the components requiring the power are contained in this one board.

Figure 10 - Schematic Diagram - ERL 310414F1

(courtesy Emhiser Research Limited)

The voltage source section of the circuit is shown at the top of the schematic. The majority of the circuit is quite straight forward (a +15V and a +5V regulated power supply). The only part of this circuit that requires much analysis is the +20V supply (for the power amplifier located elsewhere in the transmitter).

The power amp should not be turned on until the PLL establishes lock. This is even more imperative as the operating frequency is in a range specified for military use (the S Band). If the transmitter is sending out signals off frequency, there could possibly be catastrophic results.

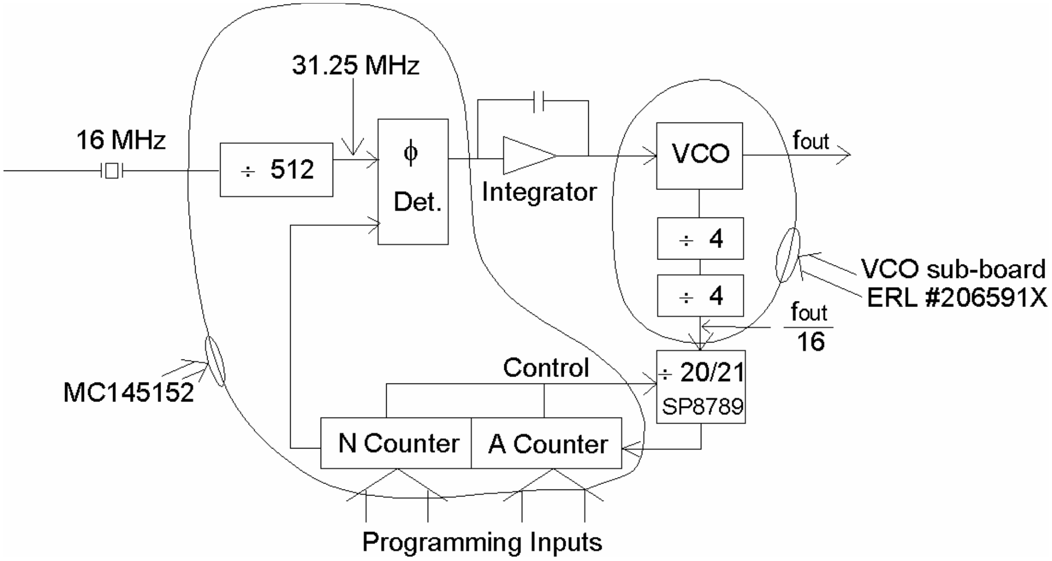
To guarantee that the +20V line does not turn on until the PLL is locked, a field-effect transistor or FET (Q5) configured as a gate follower is connected to the lock detect line of the PLL IC (U5). Whenever the PLL is locked, 5V appears at the drain of Q5 and therefore at the base of Q3 (a PNP transistor)

6.3 Frequency Synthesis

The main purpose of the 310410F is to provide an accurate frequency output (with frequency modulation - FM) that will subsequently be transmitted. This is accomplished with the use of a PLL, of which the majority is actually on the 310410F. The remainder (the VCO) is on a separate circuit board (ERL part number 206591X). The only section of the VCO board that will be mentioned in any detail are two divide-by-four blocks.

Channelized AC Telemetry Phase Lock Control Board

Figure 11 - Block Diagram - PLL in ERL 310410F



(courtesy Emhiser Research Limited)

The two circuit boards (310410F and 206591X) are connected by four wires. Two of them, the +15V and +5V lines (to power the ICs on the VCO), are 26 AWG stranded wire. The other two, VCO RF/16 and CONTROL VOLTS, are carrying the frequency from the VCO and the control voltage to the VCO respectively, and are thus more sensitive to noise. For this reason, these two connections are done with very small shielded coaxial cables.

A block diagram of the frequency synthesis PLL is shown in figure 11. The sections to be analyzed are the crystal oscillator providing the reference frequency, the divider networks, the phase lock IC (Motorola's MC145152) which contains the phase detector and the controller for the dual modulus divider (Plessey Semiconductor's SP8789) and the integrator.

6.4.1 Crystal Oscillator

The local reference frequency is generated by a modified Colpitts oscillator. The 16 MHz crystal (Y1) operates at a point where it acts as a high Q inductor to provide a resonance with the capacitors C36 and C37. The combination of C33, C34 and C35 provide a balancing effect which aligns the crystal frequency to 16 MHz.

The thermistor (R35) is of the negative temperature coefficient (NTC) variety. This means as the temperature increases, the resistance approaches 0 ohms. The effect of this is to provide a greater series capacitance to be provided by C35 as the temperature increases. This is necessary as the center frequency of the crystal changes slightly with an increase of temperature.

The output of the crystal oscillator is applied to the OSCin pin on U5 (pin 27 on the MC145152).

6.4.3 Divider Networks

To be used for frequency synthesis purposes, the PLL must also contain frequency dividers or multipliers. The use of dividers is more common as dividers are simple to manufacture (single modulus dividers can be made with flip-flops), and are more dependable than frequency multipliers.

In the 310410F, the desired output frequency is in the S band (actually between 2.200 GHz and 2.300 GHz). As it is not feasible to create a reference frequency of this magnitude, it becomes necessary to use frequency division.

The first frequency division is internal to U5 (the Phase Lock IC). It is programmed by pins four through six inclusive. This divides the frequency on pin 5 (OSCin) as provided by the crystal oscillator to a more workable value. The reference frequency of the phase detector should be set as high as possible for faster lockup times, but there is a limit (in this case 44 kHz to 46 kHz - see Appendix A for mathematical derivation). For the specifications of the transmitter to be met, the internal divider was set to divide by 512 to create a reference frequency of 31.25 kHz.

To allow the PLL to function, the output frequency must be divided by a factor of 70400 to 73600. If only single modulus dividers were used, the frequency steps would be very large (sometimes as much as 10 MHz) which is not very practical. For this reason a majority of the division must be by dual (or multiple) modulus division.

Before the VCO output reached the 310410F, it is divided by 16. This is performed by two divide by four modules located on the VCO board itself. This causes the remaining division to range from 4400 to 4600, a much more managable range.

The remaining division is performed by a dual modulus (or pulse-swallowing) counter. In the case of the 310410F, Plessey Semiconductor's SP8789, a 20/21 divider is used. The dual modulus counter is controlled by circuitry internal to the MC145152 to divide by 20 N times and by 21 A times allowing any combination of division. This allows for any division ratio between 60 and 21783 to be selected (the limits are imposed by the MC145152 IC). The frequency steps when using this circuit becomes 500 kHz which is a sight better than 10 MHz. The values of N and A are programmed by the manufacturer of the 310410F to provide the correct division ratio (to be discussed later when dealing with the MC145152)

6.4.5 Phase Lock IC (MC145152)

The phase detector, the control for the dual modulus counter (U3) and the reference frequency divider are all contained in a single package, U5. The package used on the 310410F is the MC145152FN2 which is a PLCC (Plastic Leaded Chip Carrier) device that measures approximately 1" square (25 mm square).

The phase detector in the MC145152 is a digital tri-state comparator, although of a slightly more complicated design than the one shown in figure 4. The outputs PhaseR and PhaseV (pins seven and eight respectively) are applied to the integrator in a differential manner. The behaviour of PhaseR and PhaseV are as follows: If f_{in} is greater than f_r or if the phase of f_{in} is leading, then PhaseR goes high and PhaseV pulses low. If f_{in} is less than f_r or if the phase of f_{in} is lagging, then PhaseV goes high and PhaseR pulses low. If f_{in} equals f_r and both are in phase then PhaseV and PhaseR both go high and both pulse low in phase for a minimal time[3]. These pulses are then fed to the integrator which converts them into suitable VCO control voltages.

Simultaneously, the MC145152 provides a lock detect pin (pin 28) to signal the PLL is in the locked condition. The output is analagous to the logical AND of PhaseR and PhaseV.

The control circuitry for the dual modulus divider is also internal to the MC145152. The N and A counters are loaded directly from the programmed inputs (N0-N9 and A0-A5) at the beginning of each count cycle. The controller pulls the Mod Ctrl pin (pin 9) low at the beginning of each count cycle signalling to the SP8789 (dual modulus divider) to divide by 21. The Mod Ctrl line remains low as the A counter and N counter are decremented each time a pulse enters Fin (pin 1). Once the A counter reaches zero, the Mod Ctrl line goes high signalling the SP8789 to divide by 20. This continues as the N counter is decremented on the arrival of each pulse on Fin. When the N counter reaches zero, the count cycle is over and the counters are reloaded, and the next count cycle starts. [3]

As an example of the required programming, for an output frequency of 2244.5, the N counter would be programmed to be 224 (or 0011100000 in binary) and the A counter would be programmed to 9 (or 001001 in binary) - see Appendix A for derivation. These values are programmed by connecting all of the pins that must be set to zero to ground and leaving the logic ones unconnected. The pins to be programmed are 11 through 20 for the N counter (least signifigant bit LSB to most significant bit MSB) and 23 through 25 and 10 for A (23 is LSB and 10 is MSB).

The frequency reference divider in the MC145152 has eight different divide ratios that can be selected by programming RA0-RA2 using the following code: [3]

RA2	RA1	RA0	Ratio
0	0	0	8
0	0	1	64
0	1	0	128
0	1	1	256
1	0	0	512
1	0	1	1024
1	1	0	1160
1	1	1	2048

A logic one is realized by connecting the pin to +5V and a logic zero by connecting the pin to ground.

6.4.7 Integrator

The integrator circuitry on the 310410F is virtually the same as the low-pass filter recommended in the data sheet of the MC145152. The filter is a third-order filter (whereas the recommended one was a second-order). The output of the integrator is a series of ramp functions (as the input is a series of pulses). These ramp functions make up the control voltage to the VCO.

6.5 Telemetry Modulation

The 310410F is used for AC Telemetry, so there is a more complex factor at play. The transmitter sends out an FM signal (frequency modulated - the frequency deviates slightly to encode the input data), so the lock region must be wide enough to contain the maximum deviation of the signal.

The telemetry input is first isolated from its source by use of a FET configured as a gate follower. The input is then put through a second-order passive low-pass filter (consisting of C14-C16 and R11-R13). The filter is temperature compensated (by the NTC thermistor R11) to adjust for the change in the capacitance values as temperature varies.

The telemetry modulation is then mixed with the control volt line to the VCO. Thus when the telemetry modulation signal is high, the control voltage is increased, and the VCO outputs a slightly higher frequency. When the telemetry signal is negative, the control voltage is decreased, forcing the VCO to a lower frequency.

The PLL corrects the changes caused by the telemetry as f_{in} as seen by the phase detector will be either higher or lower than the reference frequency. The output of the integrator (to the VCO) will be decreased, forcing the VCO back to the center (or carrier) frequency. This is the reason that it is referred to as AC telemetry. If the 310410F was a DC Telemetry board, there would have to be no corrective action taken by the PLL. This is far more complex than the AC coupling.

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GLOSSARY

Duty Cycle	The percent of the square wave that is in the high state

APPENDIX A - Mathematical Derivations

Section 2.1.1 [7]

Diode Ring

Input Signal: $\theta_i = A_i \sin \omega_0 t$ 1

Reference Signal: $\theta_r = A_r \sin(\omega_0 t + \phi)$ 2

Output signal:

$$\theta_e = \theta_i \theta_r = \frac{A_i A_r}{2} K \cos\phi - \frac{A_i A_r}{2} K \cos(2\omega_0 t + \phi) \quad 3$$

(K is the mixer gain)

The low pass filter is to eliminate the second harmonic before it reaches the VCO, so the output signal becomes:

$$\theta_e = \frac{A_i A_r}{2} K \cos\phi \quad 4$$

If the error signal is zero, $\theta_e = 0 = \frac{A_i A_r}{2} K \cos\phi$ 5

which reduces to: $\cos\phi = 0 \; \_ \; \phi = \frac{\pi}{2} = 90^\circ$ 6

Thus, the error signal is proportional to the phase difference from 90°

For small changes in phase:

$$\theta_e \_ \frac{\pi}{2} + \Delta\phi = \frac{A_i A_r}{2} K[\cos(\frac{\pi}{2} + \Delta\phi)] = \frac{A_i A_r}{2} K \sin\Delta\phi \quad 7$$

For very small phase change: $\theta_e \_ \frac{A_i A_r K}{2} \Delta\phi$ 8

Since the output is filtered to: $\theta_e = K_\theta(\theta_i - \theta_r)$ 9

The phase detector scale factor is: $K_\theta = \frac{A_i A_r K}{2}$ 10

For larger deviations in phase it becomes nonlinear:

$$\theta_e = K_\theta \sin\Delta\phi \quad 11$$

APPENDIX A - Mathematical Derivations (continued)

Section 3.2.2

The maximum reference frequency of the phase detector in an FM PLL is limited by the following formula:

$$f_{r\,\max} = \frac{f_o}{\left(\frac{Dev_{\max}}{\mathrm{Mod}_{\min}}\right)}$$

where:
$f_{r\,\max}$ is the maximum reference frequency
f_o is the output frequency
Dev_{max} is the maximum deviation in frequency
Mod_{min} is the minimum modulation frequency

If the reference frequency is greater than $f_{r\,\max}$, the feedback loop frequency can overtake the reference frequency. If this happens, the PLL will lose lock.

For the transmitter that the 310410F was built for, the values of the above variables are (as taken from the customer's specifications):
Dev_{max} = 1 MHz
Mod_{min} = 20 Hz

For f_o = 2200 MHz

$$f_{r\,\max} = \frac{2200x\,10^6\ Hz}{\left(\frac{1x\,10^6\ Hz}{20\ Hz}\right)} = 44x\,10^3\ Hz = 44\ kHz$$

For f_o = 2300 MHz

$$f_{r\,\max} = \frac{2300x\,10^6\ Hz}{\left(\frac{1x\,10^6\ Hz}{20\ Hz}\right)} = 46x\,10^3\ Hz = 46\ kHz$$

APPENDIX A - Mathematical Derivations (continued)

Section 3.2.3 - N Counter/A Counter Programming

For a given frequency f, the A and N counter values are as follows:

$$A = \frac{(\frac{f}{16})}{31.25\ kHz} \bmod 20 = (\frac{f}{500\ kHz}) \bmod 20$$

$$N = \frac{[\frac{\frac{f}{16}}{31.25\ kHz} - A]}{20} = \frac{\frac{f}{500\ kHz} - A}{20} = \frac{f}{10\ MHz} - \frac{A}{20}$$

For example: if f = 2244.5 MHz

$$A = (\frac{2244.5\ MHz}{500\ kHz}) \bmod 20 = 4489 \bmod 20 = 9$$

$$N = \frac{2244.5\ MHz}{10\ MHz} - \frac{9}{20} = 224.45 - 0.45 = 224$$

In order to program the MC145152, it is necessary to obtain A and N in their binary representation:

$$A = 9 = 8 + 1 = 2^3 + 2^0 = 1001_2$$

$$N = 224 = 128 + 64 + 32 = 2^7 + 2^6 + 2^5 = 11100000_2$$